AMENDMENTS TO THE CLAIMS

(currently amended) A processing system comprising:

a processor that is adapted to write compressed data;

a volatile memory device coupled to communicate with the processor over a first bus;

a non-volatile memory device, external from the volatile memory device, coupled to receive the compressed data from the processor over a second bus separate from the first bus, the non-volatile memory device further connected to transfer data to the volatile memory device over a dedicated third bus without intervention by another device; and

a decompression circuit provided in the non-volatile memory device to decompress the data being transferred to the volatile memory device.

2. (original) The processing system of claim 1 wherein the volatile memory device initiates the data transfer.

3. (original) The processing system of claim 1 wherein the non-volatile memory device is a flash memory device.

4. (original) The processing system of claim 1 wherein the processor is coupled to store compressed data in the volatile memory device.

5. (original) The processing system of claim 1 wherein volatile memory device is a dynamic random access memory.

6. (currently amended) A processing system comprising:

a processor that is adapted to write compressed data;

a synchronous memory device coupled to communicate with the processor via a synchronous first bus;

a flash memory device coupled to receive the compressed data from the processor via a serial second bus and communicate with the synchronous memory device, wherein the flash memory device is separate from the synchronous memory device and transfers data to the

synchronous memory device over a dedicated third bus without intervention by another device; and

a decompression circuit provided in the flash memory device to decompress the data while transferring to the synchronous memory device.

7. (original) The processing system of claim 6 wherein the synchronous memory device initiates the data transfer.

8. (original) The processing system of claim 7 wherein the synchronous memory device provides a system reset signal to the processor after the data is transferred from the flash memory device.

9. (original) The processing system of claim 6 wherein the synchronous memory device is an SDRAM.

10. (original) The processing system of claim 6 wherein the synchronous memory device is an RDRAM.

11 – 15 (cancelled)

16. (currently amended) A processor system power-up method, in a system having a processor coupled to a synchronous memory over a synchronous first bus and a flash memory device over a serial second bus, the synchronous memory connected to the flash memory device over a dedicated third bus, the method comprising:

detecting a power-up condition with a reset controller and providing a reset signal to ~~a~~ the synchronous memory;

using the synchronous memory, initiating a data transfer, over ~~a~~ the dedicated third bus without intervention by another device, from ~~a~~ the flash memory that is separate from the synchronous memory and that comprises a decompression capability to the synchronous memory in response to the reset signal;

using the decompression capability of the flash memory, decompressing data stored in the flash memory while transferring the data to the synchronous memory over the dedicated third bus; and

providing a system reset signal from the synchronous memory to ~~a~~ the processor after the data has been transferred.

17. (original) The method of claim 16 wherein the synchronous memory is coupled to the processor via a synchronous bus.

18. (previously presented) The method of claim 16 wherein the synchronous memory device is either an SDRAM or an RDRAM.

19. (currently amended) A method of loading a synchronous dynamic random access memory (SDRAM) in a system having a processor coupled to the SDRAM over a synchronous first bus and a flash memory device over a serial second bus, the method comprising:

using the SDRAM, initiating a data transfer from ~~a~~ the flash memory, that is separate from the SDRAM, to the synchronous dynamic random access memory over a dedicated third bus that connects only the SDRAM and the flash memory without intervention by another device; and

decompressing data stored in the flash memory while transferring the data to the synchronous dynamic random access memory; and

providing a system reset signal from the SDRAM to ~~a~~ the processor after the data has been transferred.

20. (currently amended) A method of loading a synchronous rambus dynamic random access memory (RDRAM) in a system having a processor coupled to the SDRAM over a synchronous first bus and a flash memory device over a serial second bus, the method comprising:

using the RDRAM, initiating a data transfer from ~~a~~ the flash memory, comprising a decompression capability, to the synchronous rambus dynamic random access memory in response to the reset signal, the data transfer occurring over a dedicated third bus connected only

between the flash memory and the synchronous rambus dynamic random access memory without intervention by another device;

using the decompression capability, decompressing data stored in the flash memory while transferring the data to the synchronous rambus dynamic random access memory; and

providing a system reset signal from the RDRAM to ~~a~~ the processor after the data has been transferred.